## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A dynamic sequential device comprising:

a scan circuit that allows said dynamic sequential device to be ~~scan~~ controlled and observed during a scan.

2. (Original) The dynamic sequential device of claim 1, wherein said scan circuit comprises,

an input circuit that operates to control the internal state of the dynamic sequential device; and

an output circuit that asserts a data value that represents the internal state of the dynamic sequential device, wherein said input circuit and said output circuit allow said dynamic sequential device to be scanned and controlled.

3. (Currently Amended) The dynamic sequential device of claim 2, wherein said input circuit comprises,

a pull down circuit to maintain state of a dynamic input node of said dynamic sequential device in ~~said~~ a scan state; and

a scan control circuit driven by one or more clock signals to control when said dynamic sequential device is in said scan state.

4. (Original) The dynamic sequential device of claim 2, wherein said output circuit of said scan circuit is driven by said dynamic sequential device.

5. (Original) The dynamic sequential device of claim 1, wherein said dynamic sequential device comprises one of a dynamic glitch latch and a dynamic pulse catcher.

6. (Original) A method of testing a dynamic sequential circuit capable of storing at least one bit, said method comprising the steps of:

providing said dynamic sequential circuit with a scan circuit to control and determine a state of said dynamic sequential circuit; and

controlling said scan circuit to determine said state of said dynamic sequential circuit using one or more clock signals and one or more control signals.

7. (Original) The method of claim 6, further comprising the step of determining from a data value asserted by said scan circuit if said dynamic sequential circuit is capable of storing at least one bit.

8. (Currently Amended) The method of claim ~~6~~ 7, further comprising the step of maintaining state of a dynamic input node of said dynamic sequential circuit when said scan circuit determines said state of said dynamic sequential circuit.

9. (Currently Amended) The method of claim 8, further comprising the step of precharging said dynamic input node to a known state after said scan circuit asserts said data value.

10. (Currently Amended) The method of claim 6, wherein the one or more clock signals includes a scan in clock signal and a scan out clock signal, wherein said scan in clock signal initiates said controlling of said dynamic sequential circuit and said scan out clock signal triggers said ~~test~~ scan circuit to assert said state of said dynamic sequential circuit.

11. (Original) The method of claim 6, wherein said dynamic sequential circuit comprises one of a dynamic glitch latch and a dynamic pulse catcher.

12. (Original) A method for in-circuit testing of a dynamic sequential device having a scannable test circuit, said method comprising the steps of:

controlling said scannable test circuit to determine a state of said dynamic sequential device; and

determining if said dynamic sequential device is able to operate as a dynamic sequential device based on said determined state of said dynamic sequential device.

13. (Original) The method of claim 12, further comprising the steps of:

preventing a dynamic circuit in-circuit with said dynamic sequential circuit from evaluating when said scannable test circuit determines said state of said dynamic sequential device.

14. (Original) The method of claim 13, further comprising the step of maintaining state of a dynamic input node of said dynamic sequential device when said scannable test circuit determines said state of said dynamic sequential device.

15. (Original) The method of claim 14, further comprising the step of precharging said dynamic input node to a known state before said scannable test circuit determines said state of said dynamic sequential device.

16. (Original) The method of claim 12, wherein said dynamic sequential device comprises one of a dynamic glitch latch and a dynamic pulse catcher.

17. (Original) A dynamic latch comprising:

a test circuit adapted to allow in-circuit scan testing of said dynamic latch.

18. (Original) The dynamic latch of claim 17, wherein said test circuit comprises:

an input circuit wherein said input circuit controls when said dynamic latch changes state; and

an output circuit to assert said state change.

19. (Original) The dynamic latch of claim 18, wherein said input circuit comprises,

a pull down circuit; and

a control circuit, wherein said pull down circuit and said control circuit control when said dynamic latch changes state during said in-circuit scan testing.

20. (Original) The dynamic latch of claim 18, wherein said output circuit asserts a logic level representative of an internal state of said dynamic latch, wherein said output circuit is driven by said dynamic latch to assert said logic level.